What is claimed is:

1. A test apparatus for testing a semiconductor device, comprising:

an external test unit;

a test circuit formed in the semiconductor device; and

a test device which is coupled between the external test unit and the semiconductor device, wherein pattern data for a pattern dependency test is stored in the test circuit and pattern data for a timing dependency test is stored in the test device.

2. The test apparatus according to claim 1, wherein the test circuit is a built in self test (BIST) circuit and the test device is a built out self test (BOST) device.

3. The test apparatus according to claim 2, wherein the external test unit provides a control signal to the BOST device which generates back pattern data by inverting the pattern data for the timing dependency test in accordance with the control signal.

4. The test apparatus according to claim 2, wherein the external test unit provides the BOST device with an output level generating voltage which is used to generate an output level and a reference voltage for input level decision, which is used to determine an input signal supplied from the BOST device.

5. The test apparatus according to claim 2, wherein the BIST circuit generates a signal indicative of a test result by performing a pattern dependency test on the

10073129.021302

semiconductor device using the pattern data for the pattern dependency test, and the BOST device receives the signal indicative of the test result from the BIST circuit and determines whether the test result is accurate.

6. The test apparatus according to claim 5, wherein based on a result of decision on the test result, the decision circuit provides reference data to the external test unit or generates inverted data of the reference data and provides the inverted data to the external test unit.

7. The test apparatus according to claim 5, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, and the test apparatus further comprises:

a contactor substrate for coupling the BOST device to the semiconductor device; and

a switch circuit, provided in the contactor substrate, for disconnecting the BOST device from the semiconductor device in accordance with a decision result from the decision circuit.

8. The test apparatus according to claim 5, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, the BOST device has a first surface having a first contactor, which is coupled to the semiconductor device, and a second surface having a second contactor, and the test apparatus further comprises a contactor substrate coupled to the second contactor.

9. The test apparatus according to claim 5, wherein the semiconductor device is one of a plurality of

1007129.021202

semiconductor devices arranged on a wafer, the BOST device has a first surface having a first contactor, which is coupled to the semiconductor device, and a second surface, and the test apparatus further comprises a contactor substrate adhered to the second surface.

10. The test apparatus according to claim 5, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, and the test apparatus further comprises:

a socket for retaining the BOST device; and

a contactor substrate, applied to the socket, for connecting the BOST device to the semiconductor device.

11. The test apparatus according to claim 5, wherein the BOST device includes a pattern generating circuit, coupled to the semiconductor device, for generating the pattern data for the timing dependency test and a clock signal, and the test apparatus further comprises:

a first interconnection line for supplying the clock signal to the semiconductor device from the pattern generating circuit;

a second interconnection line for connecting the semiconductor device to the decision circuit; and

a third interconnection line which has a length equal to a sum of lengths of the first and second interconnection lines and provides the clock signal to the decision circuit from the pattern generating circuit.

12. The test apparatus according to claim 11, wherein the decision circuit includes a measuring circuit for measuring an access time of the semiconductor device using an output signal from the semiconductor device and

10073129.021302

the clock signal output from the pattern generating circuit.

13. The test apparatus according to claim 12, wherein the measuring circuit includes:

a logic circuit for generating an EOR logical signal by performing an EOR operation on the clock signal and the output signal; and

a frequency counter, coupled to the logic circuit, for measuring a time interval of the EOR logical signal.

14. The test apparatus according to claim 12, wherein the measuring circuit includes:

an OR circuit for receiving an output signal of plural bits output from the semiconductor device and generating an OR logical signal;

an AND circuit for receiving an output signal of plural bits output from the semiconductor device and generating an AND logical signal;

a first frequency counter, coupled to the OR circuit, for generating a first count value in accordance with the OR logical signal and the clock signal;

a second frequency counter, coupled to the AND circuit, for generating a second count value in accordance with the AND logical signal and the clock signal; and

an access-time measuring circuit, coupled to the first and second frequency counters, for measuring an access time of the semiconductor device based on one of the first and second count values.

15. A semiconductor device comprising:

a BIST circuit in which plural pieces of test pattern data for performing a pattern dependency test are stored.

1007129.021302